Solutions - Midterm Exam

(October 20th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (22 PTS)

a) Complete the following table. The decimal numbers are unsigned: (3 pts.)

Decimal	BCD	Binary	Reflective Gray Code
50	01010000	110010	101011
128	000100101000	10000000	11000000

b) Complete the following table. The decimal numbers are signed. Use the fewest number of bits in each case: (15 pts.)

	REPRESENTATION		
Decimal	Sign-and-magnitude	1's complement	2's complement
-31	111111	100000	100001
-16	110000	101111	10000
27	011011	011011	011011
-32	1100000	1011111	100000
-1	11	110	1
-19	110011	101100	101101

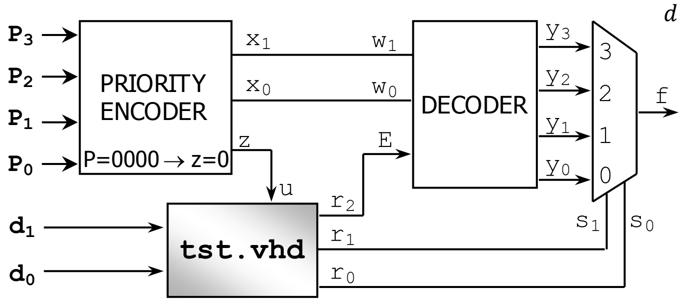
c) Convert the following decimal numbers to their 2's complement representations. (4 pts)

- ✓ -17.125
  +17.125 = 010001.001 ⇒ -17.125 = 101110.111
- ✓ 32.75
  +32.75 = 0100000.11

PROBLEM 2 (14 PTS)

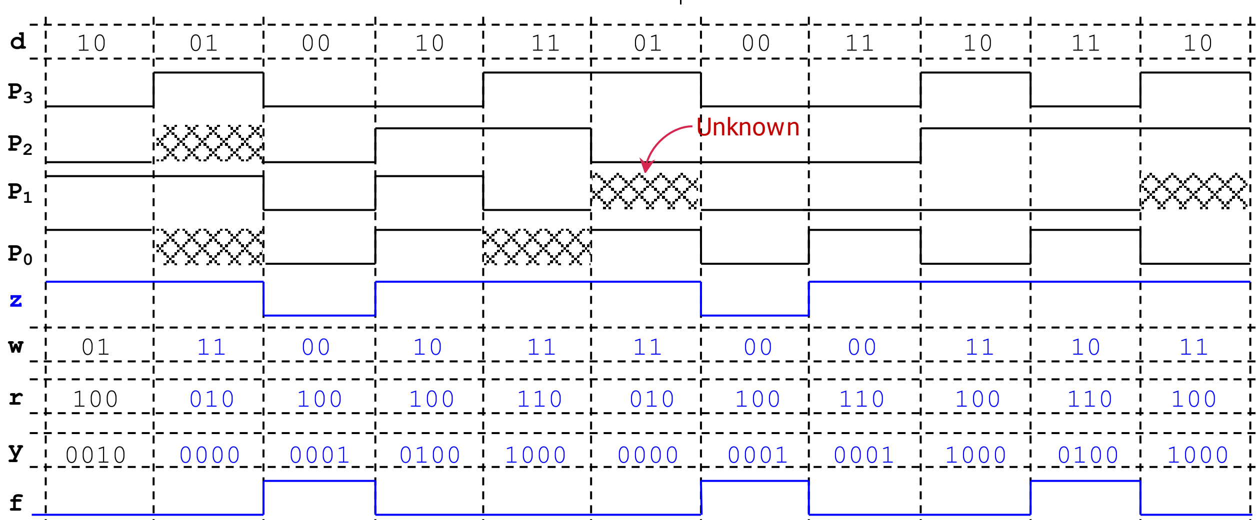
- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.

$d = d_1 d_0,\ w = w_1 w_0,\ r = r_2 r_1 r_0,\ y = y_3 y_2 y_1 y_0$



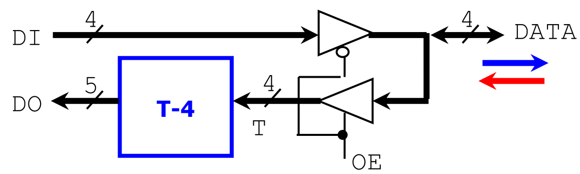

```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

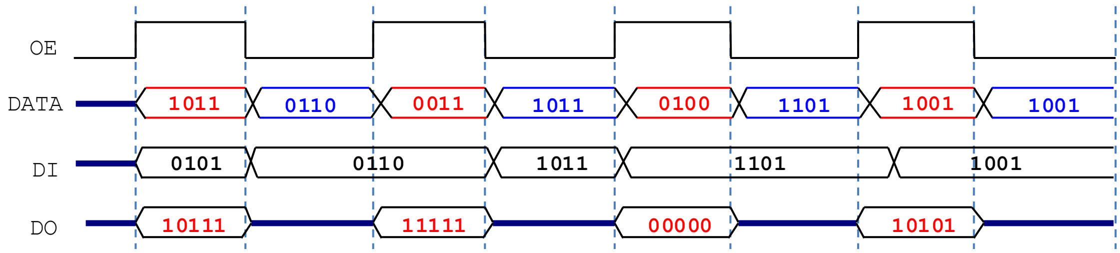
```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= '1'&d;
     if u = '1' then
        r <= d&'0';
     end if;

  end process;

end bhv;
```



PROBLEM 3 (11 PTS)

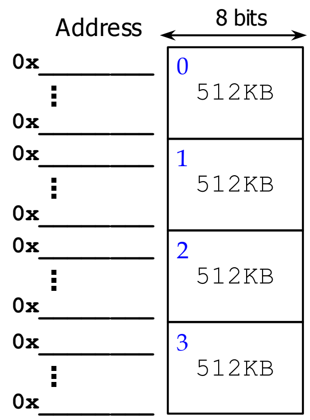
- Complete the timing diagram (signals DO and $DATA$) of the following circuit. The circuit in the blue box computes the signed operation T-4, with the result having 5 bits. T is a 4-bit signed (2C) number.
  - ✓ Example: if T=1010:
    DO = 1010 - 0100 = 11010 + 11100
    DO = 10110



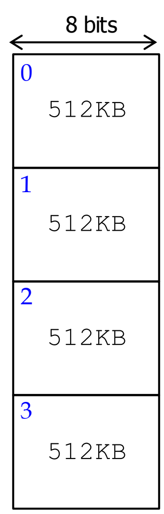


PROBLEM 4 (10 PTS)

- A microprocessor has a memory space of 2 MB. Each memory address occupies one byte. 1 KB = 2^{10} bytes, 1 MB = 2^{20} bytes, 1 GB = 2^{30} bytes.
  - ✓ What is the address bus size (number of bits of the address) of this microprocessor?
    Size of memory space: 2 MB = 2^{21} bytes. Thus, we require 21 bits to address the memory space.
  - ✓ What is the range (lowest to highest, in hexadecimal) of the memory space for this microprocessor? (1 pt.)
    With 21 bits, the address range is `0x000000` to `0x1FFFFF`.
  - ✓ The figure (right) shows four memory chips that are placed in the given positions:
    - Complete the address ranges (lowest to highest, in hexadecimal) for each of the memory chips. (8 pts)




```
                                     Address
0 0000 0000 0000 0000 0000: 0x000000
0 0000 0000 0000 0000 0001: 0x000001
   ...                       ...
0 0111 1111 1111 1111 1111: 0x07FFFF
0 1000 0000 0000 0000 0000: 0x080000
0 1000 0000 0000 0000 0001: 0x080001
   ...                       ...
0 1111 1111 1111 1111 1111: 0x0FFFFF
1 0000 0000 0000 0000 0000: 0x100000
1 0000 0000 0000 0000 0001: 0x100001
   ...                       ...
1 0111 1111 1111 1111 1111: 0x17FFFF
1 1000 0000 0000 0000 0000: 0x180000
1 1000 0000 0000 0000 0001: 0x180001
   ...                       ...
1 1111 1111 1111 1111 1111: 0x1FFFFF
```



PROBLEM 5 (15 PTS)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher bit. (6 pts)

✓ 39 + 41

```
               c6=1 c5=0 c4=1 c3=1 c2=1 c1=1 c0=0

39 = 0x27 =         1    0    0    1    1    1   +
41 = 0x29 =         1    0    1    0    0    1
---------------------------------------------------
Overflow! →    1    0    1    0    0    0    0
```

✓ 39 - 41

```
Borrow out! →  b6=1 b5=1 b4=1 b3=0 b2=0 b1=0 b0=0

39 = 0x27 =         1    0    0    1    1    1   -
41 = 0x29 =         1    0    1    0    0    1
---------------------------------------------------
                    1    1    1    1    1    0
```

b) The figure shows two 8-bit operands represented in 2's complement. Perform the 8-bit addition operation, i.e., complete all the carries and the summation bits. Also, indicate the corresponding decimal numbers for the 8-bit operands and the 8-bit result.

Does this 8-bit operation incur in overflow? Yes ~~No~~
Value of the overflow bit: $c_8 \oplus c_7 = 0$
Value of carry out bit: $c_8 = 1$

Decimal values		c_8	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0	
		1	1	0	0	0	0	0	0	0	
-41	=		1	1	0	1	0	1	1	1	+
-24	=		1	1	1	0	1	0	0	0	
-65	=		1	0	1	1	1	1	1	1	

c) Perform binary multiplication of the following numbers that are represented in 2's complement arithmetic. (4 pts)

✓ -7 x 9

```
  1 0 0 1 x        1 0 0 1 x
0 1 0 0 1    ➡     0 1 1 1
                  ---------
                   1 0 0 1
                 1 0 0 1
               1 0 0 1
             0 0 0 0
             -------------
             0 1 1 1 1 1 1
                  ⬇
             1 0 0 0 0 0 1
```

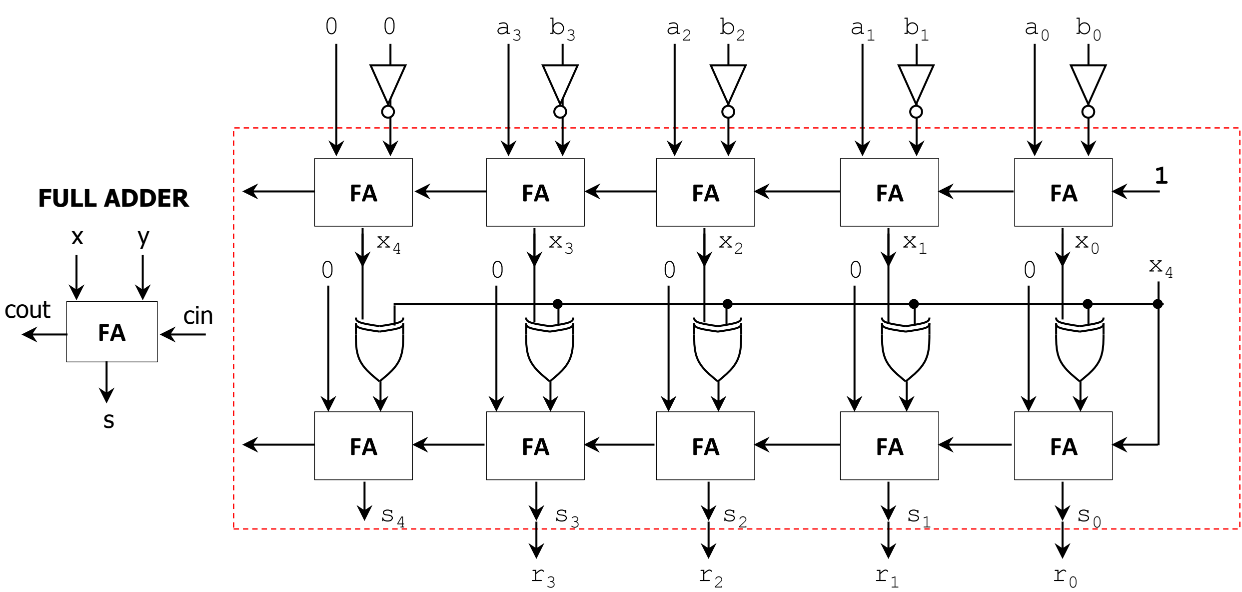
PROBLEM 6 (10 PTS)

- Sketch the circuit that computes $|A-B|$, where A, B are 4-bit unsigned numbers. For example, $A = 0101, B = 1101 \rightarrow |A-B| = |5-13| = 8$. You can only use full adders (or multi-bit adders) and logic gates. Your circuit must avoid overflow: design your circuit so that the result and intermediate operations have the proper number of bits.

$A = a_3a_2a_1a_0$, $B = b_3b_2b_1b_0$

$A, B \in [0,15] \rightarrow A, B$ require 4 bits in unsigned representation. However, to get the proper result of $A-B$, we need to use the 2C representation, where A, B require 5 bits in 2C.

- ✓ $X = A - B \in [-15,15]$ requires 5 bits in 2C. Thus, we need to zero-extend A and B to convert them to 2C representation.
- ✓ $|X| = |A-B| \in [0,15]$ requires 5 bits in 2C. Thus, the second operation $0 \pm X$ only requires 5 bits.
  - If $x_4 = 1 \rightarrow X < 0 \rightarrow$ we do $0 - X$.
  - If $x_4 = 0 \rightarrow X \geq 0 \rightarrow$ we do $0 + X$.
- ✓ $R = |A-B| \in [0,15]$ requires 5 bits in 2C. Note that the MSB is always 0. The unsigned result only requires 4 bits.



PROBLEM 6 (18 PTS)

- Sketch the circuit that implements the following Boolean function: $f(a,b,c,d) = (c \oplus d)(\overline{a \oplus b})$
  - ✓ Using <u>ONLY</u> 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (12 pts)

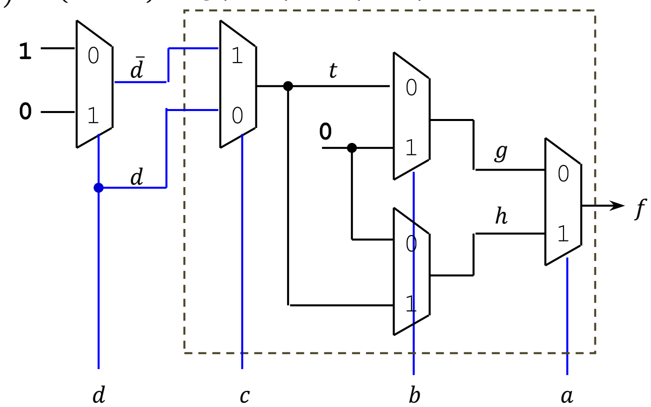
$f(a,b,c,d) = \bar{a}f(0,b,c,d) + af(1,b,c,d) = \bar{a}\left(\bar{b}(c \oplus d)\right) + a\left(b(c \oplus d)\right) = \bar{a}g(b,c,d) + ah(b,c,d)$

$g(b,c,d) = \bar{b}g(0,c,d) + bg(1,c,d) = \bar{b}(c \oplus d) + b(0)$

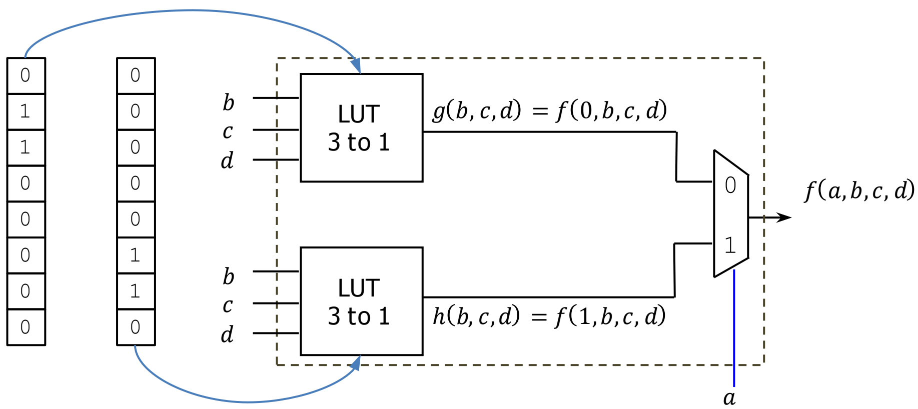
$h(b,c,d) = \bar{b}h(0,c,d) + bh(1,c,d) = \bar{b}(0) + b(c \oplus d)$

$t(c,d) = c \oplus d = \bar{c}t(0,d) + ct(1,d) = \bar{c}(d) + c(\bar{d})$

Also: $\bar{d} = \bar{d}(1) + d(0)$



  - ✓ Using two 3-to-1 LUTs and a 2-to-1 MUX. Specify the contents of each of the 3-to-1 LUTs. (6 pts)



a	b	c	d	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0